

## INF1022 Series

### 60mm DDS Digital Linear Fader

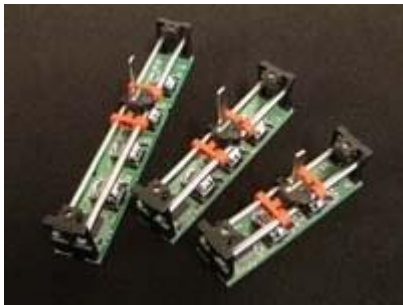
#### FEATURES

- No contact noise
- Wear life in excess of 4,000,000 cycles
- Low operational force
- Operator adjustable feel
- Eddy current damping
- Direct Digital Sampled (DDS) outputs : simplifies system design and architecture
- Self sampled device : low system processing overheads possible
- UART, SPI and analogue outputs
- High sample rate
- Easy to integrate and maintain
- Low current
- Low cost

#### APPLICATIONS

- Channel Fader
- Audio Mixers
- Speed Controls
- Positional Controls
- Lighting Desks
- Video Mixers
- Replacement for carbon track parts
- Linear Position Sensor

#### PRODUCT IMAGE



#### SUPPLY OPTIONS

From the outset, **infinium** has sought to develop and deliver a product that helps to meet its customers' commercial objectives. A key tool to deliver on this ambition is the different supply options. In summary, each product in the range can be supplied as either a fully assembled product or as a kit of mechanical parts.

The first option is for companies who are looking for an out-of-the-box solution. The fader is supplied fully assembled (mechanics and electronics). Its connector allows easy connection to the main PCB.

The second option is for companies who are looking to integrate the fader electronics into their own electronics and PCB. This option also allows the mechanics to be assembled at the customers' production facilities. Since this saves on required electrical components and assembly, it is significantly cheaper.



**DEVICE SPECIFICATIONS**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Absolute Maximum Ratings***(T<sub>A</sub> = 25°C unless otherwise specified)*

Operational Temperature	0 °C to +45 °C
Storage Temperature	-10°C to +70oC
Supply Voltage	3.60V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V <sub>DD</sub>	Guaranteed by design	3.0	3.3	3.6	volts
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> = 3.3V		9.6	11	mA
Spatial Resolution		Absolute encoder end to end		0.39		mm/step
Resolution, Counts			128			Steps
Noise Free Resolution	N <sub>FR</sub>		7			Bits
Sample Rate	F <sub>SAMPLE</sub>			1000		kHz
Startup Time	T <sub>SU</sub>	Power on to data output ready.	3.0	3.2	4.0	ms
Status Pin Drive Current	I <sub>STAT</sub>	V <sub>DD</sub> = 3.3V		8		mA
SPO leakage current	I <sub>Z</sub>	/SS = V <sub>DD</sub> , or SPI disabled, SPO open cct		10	20	uA
Low Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA; V <sub>DD</sub> = 2.4 V to 3.6 V		0.2	0.4	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -3.2 mA; V <sub>DD</sub> = 2.4 V to 3.6 V	V <sub>DD</sub> - 0.7	V <sub>DD</sub> - 0.4		V
Low Level Input Voltage	V <sub>IL</sub>	V <sub>DD</sub> = 2.4 V to 3.6 V	-0.5		0.3V <sub>DD</sub>	V
High Level Input Voltage	V <sub>IH</sub>	V <sub>DD</sub> = 2.4 V to 3.6 V	0.7V <sub>DD</sub>		5.5	V
Capacitance	C	Any pin to 0V			30	pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analogue Output Zero	A <sub>ZERO</sub>	V <sub>DD</sub> = 3.3V	0		0.1	V
Analogue Output Fullscale	A <sub>FS</sub>	V <sub>DD</sub> = 3.3V	V <sub>DD</sub> - 0.1		V <sub>DD</sub>	V
Analogue Output Impedance	Z <sub>A</sub>	V <sub>DD</sub> = 3.3V	20	22	24	Kohm
Analogue Time Constant	A <sub>TC</sub>	V <sub>DD</sub> = 3.3V, time to 50% of final value		3.0	3.5	ms
Analogue output error		Deviation from monotonic		± 0.25		LSB





## SPI Slave Timing

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Interval	$S_{INT}$		1.10	1.30	1.35	us
StartUp Time	$t_{SU}$	Power on to SPI data ready	3.0	3.2	4.0	ms
SPI Clock Input Frequency	$F_{SPI}$	Slave mode	0		1.198	MHz
SPI cycle time	$t_{SPICYC}$	Slave mode	835			ns
SPI enable lead time	$t_{SPILEAD}$	/SS timed slave	246			ns
SPI enable lag time	$t_{SPILAG}$	/SS timed slave	246			ns
SPICLK HIGH time	$t_{SPICLKH}$	Slave Mode	417			ns
SPICLK LOW time	$t_{SPICLKL}$	Slave Mode	417			ns
SPI data setup time	$t_{SPIDSU}$		104			ns
SPI data hold time	$t_{SPIDH}$		104			ns
SPI access time (slave)	$t_{SPIA}$		0		88	ns
SPI disable time (slave)	$t_{SPIDIS}$		0		168	ns
Clock to SPI output data valid	$t_{SPIDV}$		-		168	ns
SPI output data hold	$t_{SPIOH}$		0			
SPI rise time	Inputs	$t_{SPIR}$	SPICLK, MOSI, /SS		96	ns
	Outputs		MISO		1996	ns
SPI fall time	Inputs	$t_{SPIF}$	SPICLK, MOSI, /SS		104	ns
	Outputs		MISO		2004	ns

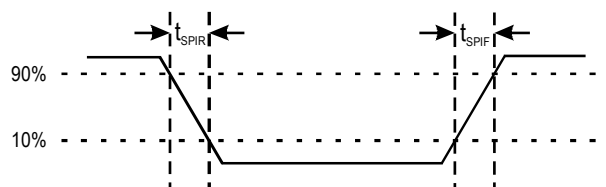


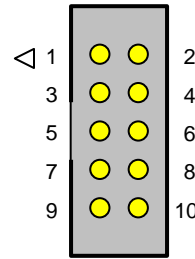
Figure 1 : SPI Rise and Fall Times





**DEVICE PIN OUT**

Pin	Function	Pin	Function
1	V <sub>dd</sub>	2	IF0
3	DC1 OUT	4	IF1
5	Reserved	6	IF2
7	GND	8	IF3
9	GND	10	/RESET



PCB header  
Viewed from  
mating side

<b>VDD</b>	Fader power, Nominally 3V3.
<b>IF0..IF3</b>	Device configuration and digital interface pins. The device mode is read on reset and then these pins take on a function specified by the mode. See Operating Mode Selection for more details.
<b>DC1 Out</b>	The analogue output pin. When selected for analogue mode and the device is not muted this pin will output a voltage between 0 and V <sub>dd</sub> proportional to the position of the fader.
<b>/RESET</b>	Active low reset signal to the fader. This signal may be used to force a reset of the fader processor if necessary

**OPERATING MODE SELECTION**

The operating mode of the fader is determined during a reset or power-up event. Pins IF0 through IF3 are used to signal the required mode. During reset these signals are inputs which are read by the fader. After the mode has been determined these pins are reconfigured for the data transfers requested. For this reason the configuration must be performed using “soft logic” states which are achieved by using pull up or pull down resistors. The circuitry on the fader features 100KΩ pull down resistors and this should be taken into account when designing the mode selection circuitry. An alternative approach is to present hard driven logic states to the INF pins during the reset and then to remove these states before the fader begins the programmed operation. The device has small series resistors fitted between the configuration pins and its processor to prevent damage to it in the event of bus contention.

MODE	Power On Logic Levels to set mode	
	IF 0	IF 1
Analogue	0	0
UART	0	1
SPI	1	0
Reserved	1	1

MODE	Pin Function after configuration			
	IF 0	IF 1	IF 2	IF 3
Analogue	Fader Status LED drive		Reserved	Reserved
UART	Tx Data	Rx Data	A0	A1
SPI	/SS	SCLK	SDI	SDO

0 = Not Connected  
1 = 10KΩ Pull-up to 3V3  
Please contact factory for details of UART mode





**FADER STATUS INDICATION**

Fader Condition	LED Drive status	
	IF2	IF3
Normal	ON	OFF
Row Error Code	ON	ON
Uncertain	OFF	OFF
Uncertain	OFF	ON

The fader provides a pair of led drive outputs to indicate its operating condition if required. To use the LED status indicators high efficiency (2 to 8mA) LEDs should be connected between the drive signal required and 0V. The LED anode should connect to the drive output signal.

**ANALOGUE MODE**

**NOTE**

*Analogue mode is only possible when using the analogue/digital output version of the fader part number INF102 XXX 2XX*

This mode is entered by default if no additional pull-up resistors are added to the IF pins at power-up or reset. The output range is from 0 to VDD with DC1 increasing linearly as the fader position increases.

The fader generates its dc output via a filtered pulse width modulated (PWM) output from the on board processor. A measurement is made of the fader position and this is used to program the PWM output.

The PWM signal operates with a fixed frequency and variable duty cycle that can be adjusted from fully off to fully on with high resolution. When this PWM signal is passed through the low-pass filter formed by the resistor and capacitor combination R22 and C7 shown opposite. The result is an analogue output that varies linearly with the fader position from 0V to the processor supply voltage, 3.3V(typically).

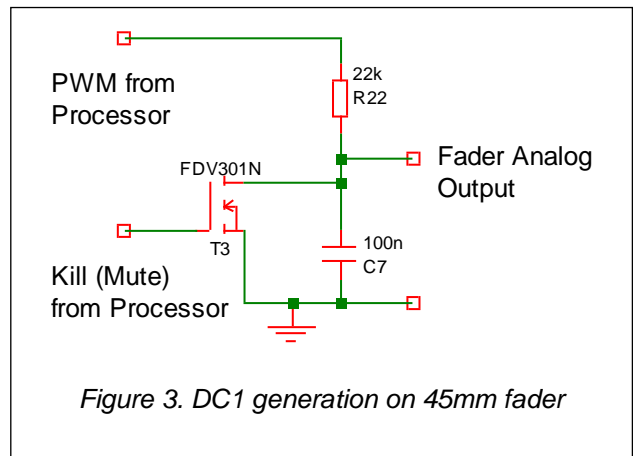


Figure 3. DC1 generation on 45mm fader

To allow a fast “Mute” or switching to minimum output of the analogue signal the DMOS F.E.T. T3 is connected directly across the capacitor, C7. When the processor switches the F.E.T. gate to a high level then the transistor conducts with a low drain source resistance which serves to discharge the capacitor quickly. Simultaneously, the PWM output is switched off in the low state with the result that the analogue output becomes 0V.

As the filter contains the high impedance element R1 it is important than any following electronics do not load this output, or the full-scale voltage swing will be reduced.

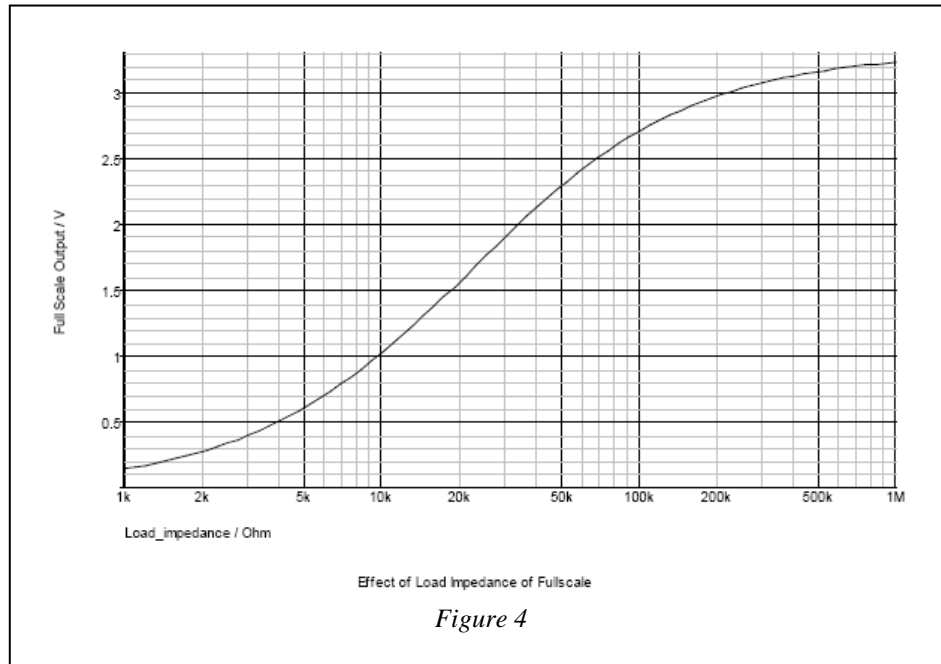
To estimate the effective output range the following formula may be used:

$$OutputRange = \frac{3.3 * Zi}{(Zi + 22000)}$$

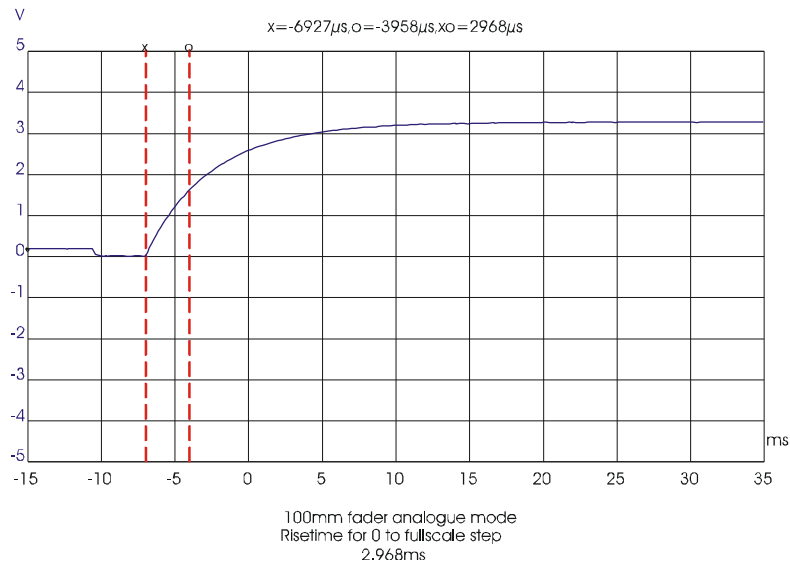
Where Zi is the input impedance of the electronics connected directly to the fader output.

This is shown graphically in figure 4





The filter components within the analogue mode PWM demodulator create a short time constant delay when a step change is made to the fader position. This response is shown below.





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**SPI MODE - SLAVE**

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The fader is configured for SPI slave operation by pulling IF1 to 3V3 via a 10KΩ resistor during power on or a reset.

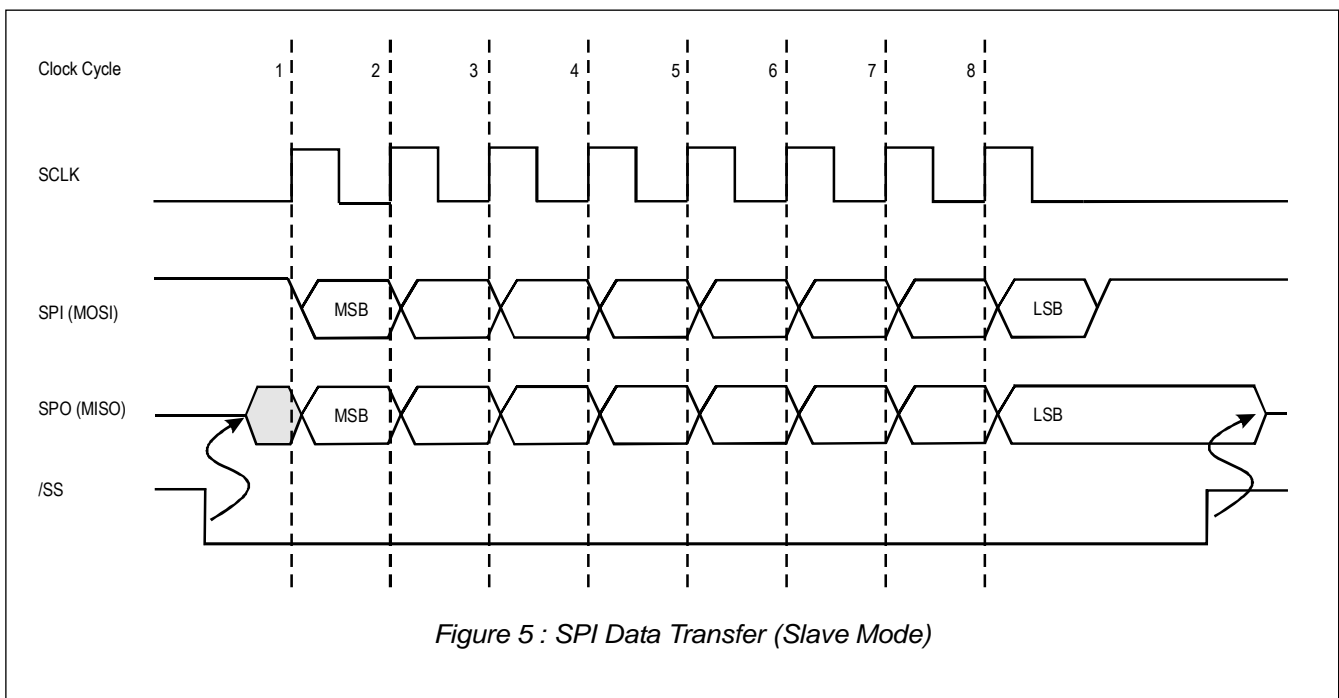
The four standard SPI signals are used for communication with the device.

- /SS : Serial Select pin, active low
- SCLK : Serial clock. Data is shifted out and latched in on rising and falling edges of the clock.
- SDI : Equivalent to MISO. Data is received into the device on this pin.
- SDO : Equivalent to MISO. Data is transmitted from the device on this pin.

The /SS signal must be cycled between each byte read of the fader for proper operation. Figure 5 shows the relationship of data in and out of the device to the clock.

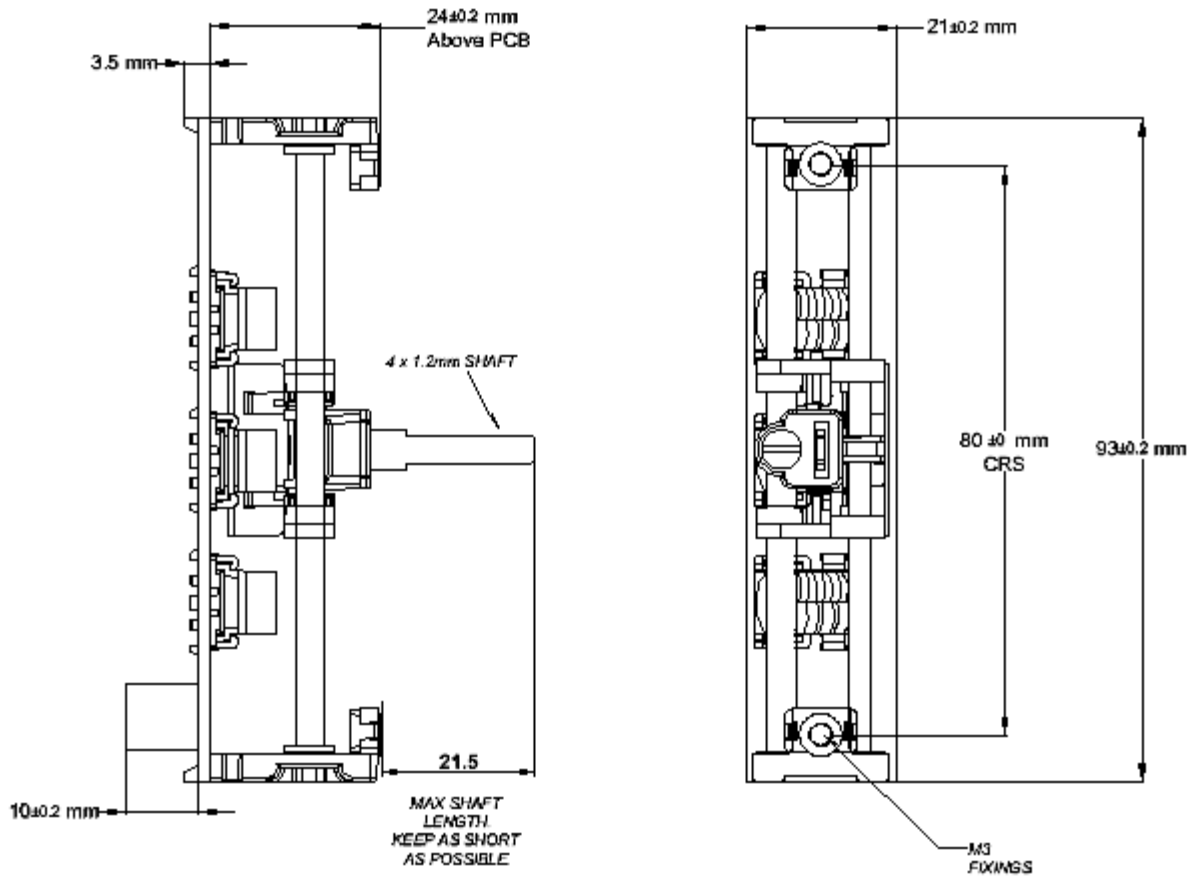
The data format is MSB first and consists of two bytes of information. The first byte contains the decoded device position as an 8 bit value that represents the number of resolution steps that the centre of the slider is from the zero position. Currently the second byte is reserved for error checking. Contact the factory for more details.

To guard against a read of the device before the SPI data is ready it is recommended that the host processor write a dummy value sequence to the fader during the read. Should this data be obtained from the fader in the next read then it can be determined that the data was not updated by the fader and so a retry should be made.





MECHANICAL DATA



The device connector is IDC Style 5 x 2 row header, 0.1" pitch intended for cable connection.





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